

# **MG82F6P32 Evaluation Board**

## **Explanation Manual**

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## 1. MG82F6P32 Features

- 1-T 80C51 Central Processing Unit
- **MG82F6P32** with **32K** Bytes flash ROM
  - ISP memory zone could be optioned as **0.5KB/1.0KB~7.5KB**
  - Flexible IAP size by software configured
  - Code protection for flash memory access
  - Flash write/erase cycle: 20,000
  - Flash data retention: 100 years at 25°C
  - **Default MG82F6P32 Flash space mapping**
    - \* AP Flash default mapping (29.5KB, 0000h~75FFh)
    - \* IAP Flash default mapping (1.0KB, F600h~F9FFh)
    - \* ISP Flash default mapping (1.5KB, FA00h~FFFFh), ISP Boot code
- Data RAM: **2K** Bytes
  - On-chip 256 bytes scratch-pad RAM
  - **MG82F6P32 - 1792** bytes expanded RAM (XRAM)
  - Support page select on XRAM access
- Dual data pointer
- Provide one channel DMA engine
  - P2P, M2P, P2M
  - Memory target: on-chip XRAM
  - Peripheral target: UART0/1, SPI, TWI0/I2C0, I2C1, ADC12 & CRC16/32
  - Timer 5 and Timer 6 are used for DMA, but it also can be traded as independent timer when DMA not in use
- Interrupt controller
  - **21** sources, four-level-priority interrupt capability
  - **Four** external interrupt inputs, nINT0, nINT1, nINT2 and nINT3 with glitch filter
  - All external interrupts support High/Low level or Rising/Falling edge trigger
  - AC0, AC1, OPA0 and OPA1 support MCU wakeup from Power Down mode
- Total **12/14** (with split mode) timers in **MG82F6P32**
  - RTC Timer and WDT Timer
  - Timer 0, Timer 1, Timer 2 and Timer 3
  - PTM0 (PWM Timer 0), PCA1 (Program Counter Array 1)
  - S0 BRG and S1 BRG
  - Timer 5/6 of DMA module also can be used as timer
  - If Timer 2/3 in split mode, **MG82F6P32** has total **14** timers
- **6** 16-bit timer/counters, Timer 0, Timer 1, Timer 2, Timer 3, Timer 5 and Timer 6
  - X12 mode and timer clock output function
  - New **6** operating modes in Timer 2/3 with 8 clock sources and 8 capture sources
  - Timer 2/3 can be split to two 8-bit timers
  - Clock Count Output (CCO) on T2CKO, T3CKO
  - Timer 0~3 support PWM mode
  - Timer 2/3 support Duty Capture function
- **One** 16-bit PWM Timer (PTM0)
  - PTM0 has 6 CP (Compare/PWM) modules
  - Reloadable 16-bit base counter to support variable length PWM
  - Up to **96MHz** clock source from on-chip CKM
  - 16-bit software timer mode and High-speed output mode
  - Variable 8/10/12/16-bit PWM mode, the PTM0 can be configured to:
    - \* Up to **6** channels un-buffered 10/12/16-bit PWM, or
    - \* Up to **6** channels buffered 2~8-bit PWM for various frequency setting, or
    - \* Up to **3** channels buffered 9~16-bit PWM for various frequency setting

- PWM with dead-time control, break control and central-aligned option
- **One** Programmable 16-bit counter/timer Arrays (PCA1)
  - PCA1 has 2 CCP (Capture/Compare/PWM) modules
  - Reloadable 16-bit base counter to support variable length PWM
  - Up to **96MHz** clock source from on-chip CKM
  - Capture mode, 16-bit software timer mode and High-speed output mode
  - Buffered capture mode to monitor narrow pulse input
  - Variable 8/10/12/16-bit PWM mode, the PCA1 can be configured to:
    - \* Up to **2** channels un-buffered 10/12/16-bit PWM, or
    - \* Up to **2** channels buffered 2~8-bit PWM for various frequency setting, or
    - \* Up to **1** channel buffered 9~16-bit PWM for various frequency setting
  - PWM with dead-time control, break control and central-aligned option
- Timer2/3, PTM0 and PCA1 has global control for output signal synchronization
- 8 Inputs Keypad Interrupt (KBI)
- 12-Bit Single-ended ADC
  - Programmable throughput up to **500K** sps
  - **MG82F6P32** has **8** channel external inputs and **5** channels for internal reference voltage (IVR/2.4V), PGAO, OP0O, OP1O, 1/4VDD and internal VSS
  - Support window detect function on ADC result
  - Support channel scan mode
  - ADC VREF+ from internal IVR 2.4V
- On-chip voltage reference (IVR 24)
- 2 Operational Amplifiers OPA (OPA0/ OPA1)
  - Low input offset, 0.5mV ~ 1mV after calibration, 3mV factory trimmed.
  - Internal 1.2V reference on positive and negative input option to be DC bias or used for offset calibration
  - Support Input and Output I/O
  - PGA output on negative input as pre-amplifier.
  - Internal output path connects to ADC and AC0 input
  - Software offset calibration with 6-bit trimming range.
  - Low power mode
  - Support comparator mode
  - Comparator mode support interrupt and can be used under power down for edge wakeup trigger source.
- Programmable Gain Amplifier (PGA)
  - Low input offset, 0.5mV ~ 1mV after calibration, 3mV factory trimmed.
  - Support Input and Output I/O
  - Gain: x1, x2, x4, x8, x16, x32, x64, x128
  - Low power mode
  - Software offset calibration with 6-bit trimming range.
- Analog Comparator 0 (AC0)
  - Selectable internal voltage reference (IVR/2.4V) on ACNIO
  - **4** selectable ACPI0(+) inputs
  - Support OPAn output to ACPI0/ACNIO for the signal comparison
  - Wake-up from power-down and idle
  - Glitch filter option and output to internal timer capture
  - Hysteresis Voltage: 0mV,  $\pm 10\text{mV}$ ,  $\pm 20\text{mV}$  and  $\pm 60\text{mV}$
  - 6 Bits Offset trimming
- Analog Comparator 1 (AC1)
  - Selectable internal voltage reference (IVR/2.4V)
  - Wake-up from power-down and idle
  - Glitch filter option and output to internal timer capture
  - Hysteresis Voltage: 0mV,  $\pm 10\text{mV}$ ,  $\pm 20\text{mV}$  and  $\pm 60\text{mV}$

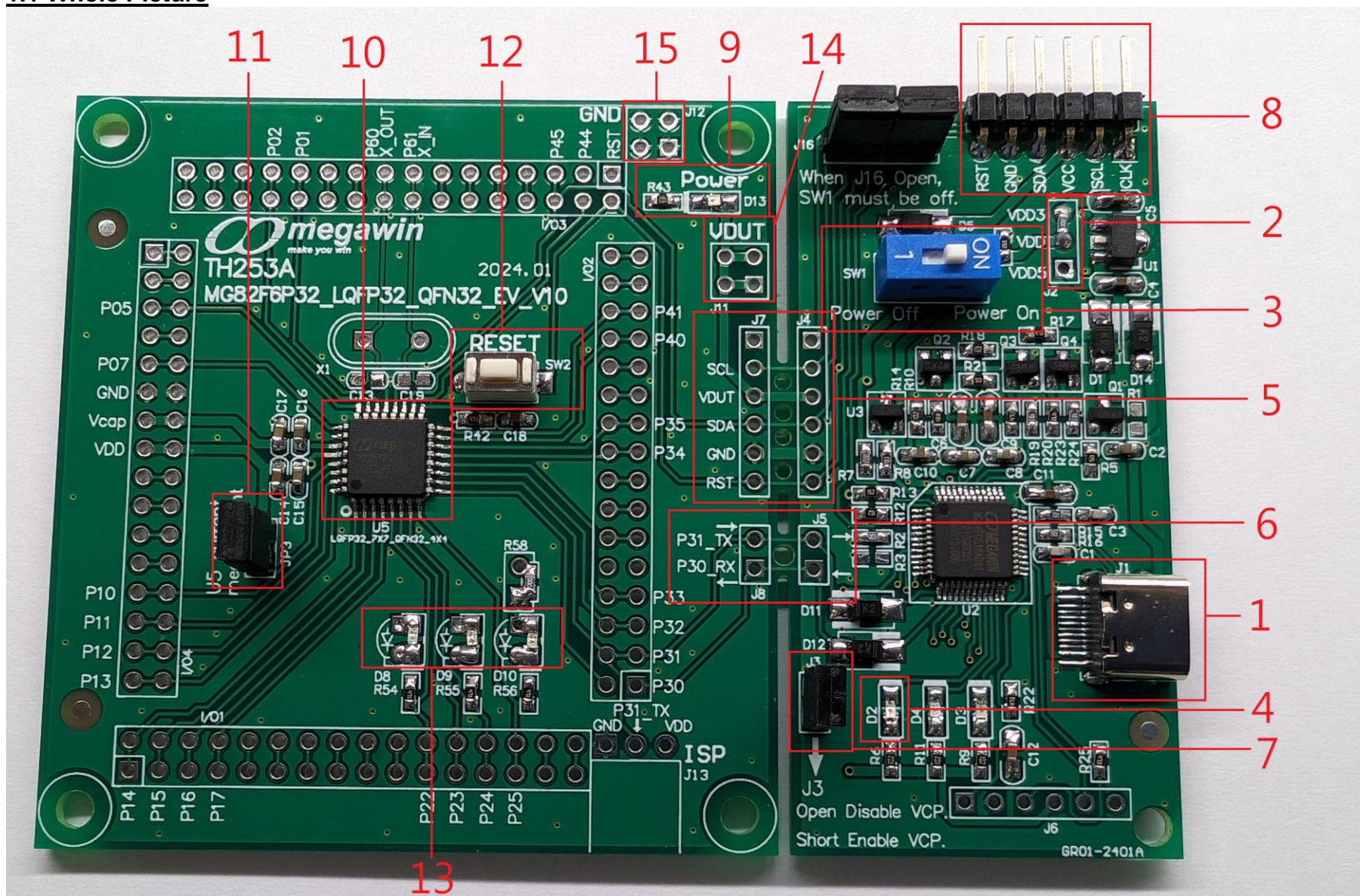
- 6 Bits Offset trimming
- Enhanced UART (S0)
  - Framing Error Detection
  - Automatic Address Recognition
  - Max. UART baud rate up to 6MHz
  - Support SPI Master in Mode 4, up to 12MHz on SPICLK
  - Built-in baud rate generator (S0BRG) to support TX or RX on different baud rate
  - S0BRG in timer mode cascaded with Timer 0/1 to be a 16/24-bit timer/counter
  - Support ARGB data transition
- 2<sup>nd</sup> UART (S1)
  - Max. UART baud rate up to 1.8432/3.0MHz
  - Support SPI Master in Mode 4, up to 12MHz on SPICLK
  - Provide BMC ENDEC for USB PD application
  - Support ARGB data transition
- One Master/Slave SPI serial interface
  - Max. 24MHz SPICLK on SPI master
  - Max 12MHz on SPI slave
  - Up to 3 SPI masters including S0/S1 in mode 4
  - Support daisy-chain function in SPI slave mode (mode 1)
- Three Master/Slave two wire serial interfaces: TWI0/I2C0, TWI1/I2C1 and STWI (SI2C)
  - Two Master/Slave hardware engine: TWI0/I2C0 and TWI1/I2C1
  - Max. 1MHz on I2C0/I2C1 master mode and Max. 400KHz on I2C0/I2C1 slave mode
  - One software TWI/I2C, STWI/ SI2C, Start/Stop serial interface detection (SID)
  - Multiple slave address recognition on I2C0/I2C1
- Programmable Watchdog Timer (WDT), clock sourced from ILRCO, XTAL or SYSCLK/12
  - One time enabled by CPU or power-on
  - Interrupt CPU or Reset CPU on WDT overflow
  - Support WDT function in power down mode (watch mode) for auto-wakeup function
- Real-Time-Clock (RTC) module, clock sourced from XTAL, ILRCO, WDTPS, WDTOF, SYSCLK or SYSCLK/12
  - Programmable interrupt period from mini-second wakeup to minute wakeup
  - 21-bit length system timer
- Beeper function
- General purpose logic (GPL/CRC)
  - Bit order reversed function
  - 16-bit CRC engine (polynomial: **0x1201**)
  - Support automatic CRC of flash content
  - Programmable initial seed function of CRC
  - 4b5b encoder/decoder (ENDEC)
  - 32-bit CRC engine (polynomial: **0x04C1\_1DB7**)
- On-Chip-Debug interface (OCD)
- Maximum **29/25** GPIOs in **32/28**-pin package
  - All I/O is Analog I/O mode as default
  - P3 can be configured to quasi-bidirectional, push-pull output, open-drain output and input only
  - P0, P1, P2, P4 and P6 can be configured to open-drain output or push-pull output
  - P6.0, P6.1 and P4.7 shared with XTAL2, XTAL1 and **nRST**
  - Programmable GPIO driving strength and driving speed
  - On chip pull-up enabled on each pin
- Clock Sources
  - Internal 12MHz/11.059MHz oscillator (IHRCO): factory calibrated to  $\pm 1\%$ , typical
  - External crystal mode, support 32.768KHz oscillating and missing clock detection (MCD)
  - Internal Low power 32KHz RC Oscillator (ILRCO)

- External clock input (ECKI) on P6.0/XTAL2, up to 25MHz
- Internal RC Oscillator output on P6.0/XTAL2
- On-chip Clock Multiplier (CKM) to provide high speed clock source **96MHz**
- Two Brown-Out Detectors
  - BOD0: detect **1.7V**
  - BOD1: selected detection level on 4.2V/**3.6V**/2.4V/2.0V
  - Interrupt CPU or reset CPU
  - Wake up CPU in Power-Down mode (BOD1)
- Multiple power control modes: idle mode, power-down mode, slow mode, sub-clock mode, RTC mode, watch mode and monitor mode.
  - All interrupts can wake up IDLE mode
  - **19** sources with **23** pins to wake up Power-Down mode
  - Slow mode and sub-clock mode support low speed MCU operation
  - RTC mode supports RTC to resume CPU in power down
  - Watch mode supports WDT to resume CPU in power down
  - Monitor mode supports BOD1 to resume CPU in power down
- Operating voltage range: 1.8V – 5.5V
  - Minimum **1.8V** requirement in flash write operation (ISP/IAP/ICP)
- Operation frequency range: **32MHz** (max)
  - External clock input mode, 0 – 12MHz @ 2.0V – 5.5V, 0 – 25MHz @ 2.4V – 5.5V
  - CPU up to 12MHz @ **1.8V** – 5.5V, and up to 25MHz @ **2.2V** – 5.5V
  - **CPU up to 32MHz @ 2.7V -5.5V with on-chip CKM**
  - **Peripheral Clock (SYSCLK) up to 48MHz**
- 16-Bytes Unique ID code
- Operating Temperature:
  - Industrial (-40°C to +105°C)\*
- Package Types:
  - LQFP32 (7 x 7 mm): MG82F6P32AD32 (32K)
  - QFN32 (4 x 4 x 0.55 mm): MG82F6P32AZ32 (32K)
  - SSOP28 (150 mil): MG82F6P32AL28 (32K)

\*: Tested by sampling.

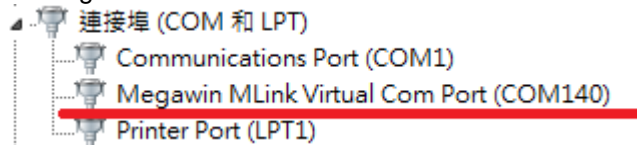


## 1.1 Whole Picture



## 1.2 Ev Board Hardware Instruction

1. J1: Type-C USB Connector.
2. J2: Power select.
  - a. VDD5 – USB 5V Output.
  - b. VDD – Select 5V or 3.3V to MG82F6P32.
  - c. VDD3 -- On Board LDO 3.3V Output(U1).
3. SW1: Control U5 power on/off.
4. D2: PC identify MLink successful when D2 turn ON.
5. J4: Connector in ICE adaptor(MLink) for connecting with EV board to program MG82F6P32.  
J7: Connector in EV board for connecting with ICE adaptor(MLink).
6. J5: Connector in ICE adaptor(MLink) for connecting with EV board to transfer UART data.  
J8: Connector in EV board for connecting with ICE adaptor(MLink).
7. J3: Virtual Com Port function selection, when J3 open and plug out → plug in PC, VCP function is disable. when J3 short and plug out → plug in PC, VCP function is enabled. After installing driver(how to install driver, refer the [2. Driver Install](#)), Device Manager will appear “Megawin MLink Virtual Com Port” as below figure.



“Megawin MLink Virtual Com Port” support as below as baud rate only:

**600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 128000, 7200, 14400, 28800...**etc bps.

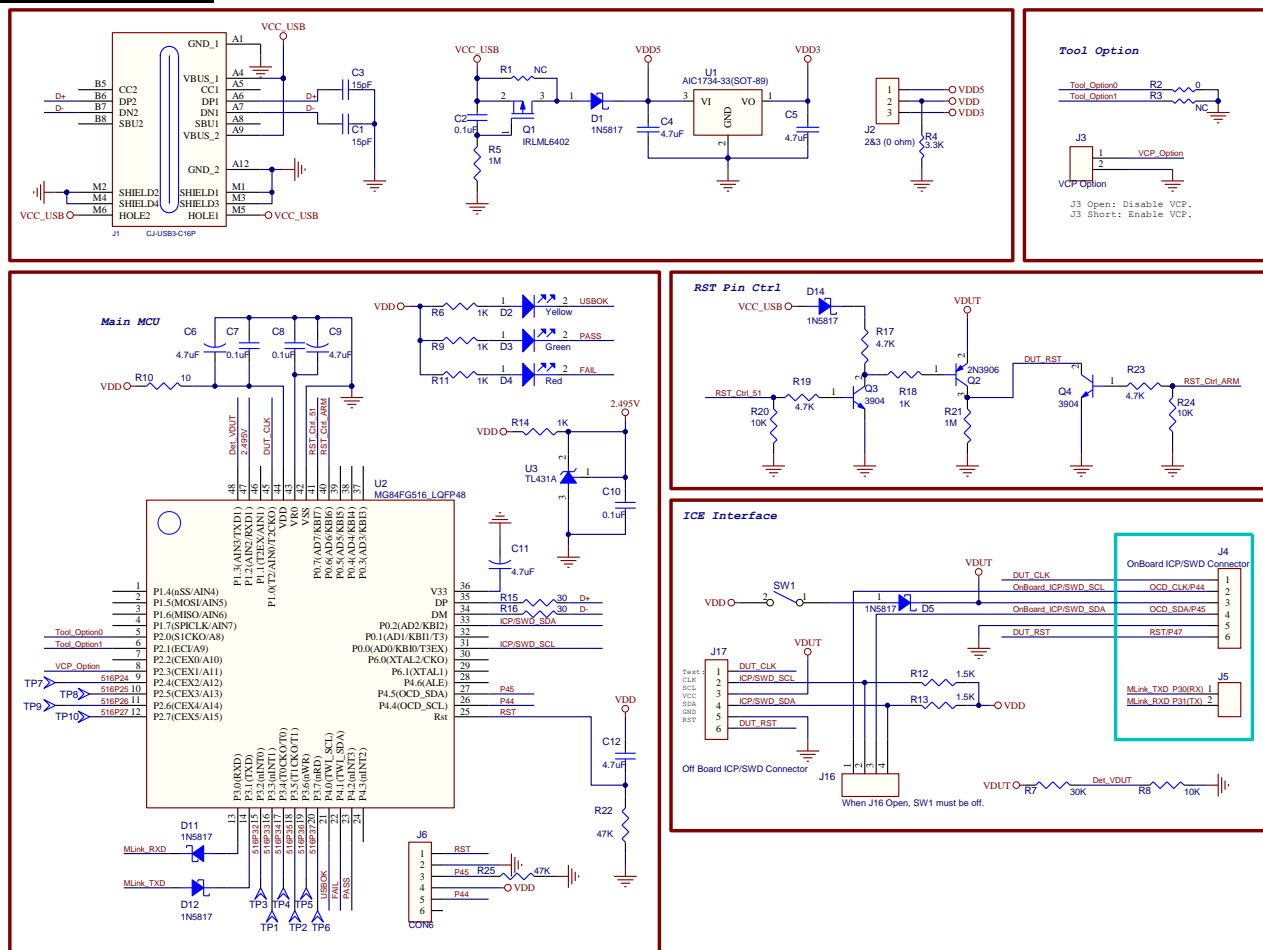
“Megawin MLink Virtual Com Port” also support **Stop Bit 1** only.

8. J17: When J16 open and SW1 off, MLink can program other DUT board through J17 connector.
9. D13: EV board power indicator LED.
10. U5: MG82F6P32 LQFP-48 package.
11. JP3: User can measure MG82F6P32 operating current by connecting an ammeter.
12. SW2: Pressing the button will trigger external reset signal to U5(MG82F6P32).
13. D8, D9, D10: IO LED.
14. J11: EV board VDUT connector.
15. J12: EV board GND connector.

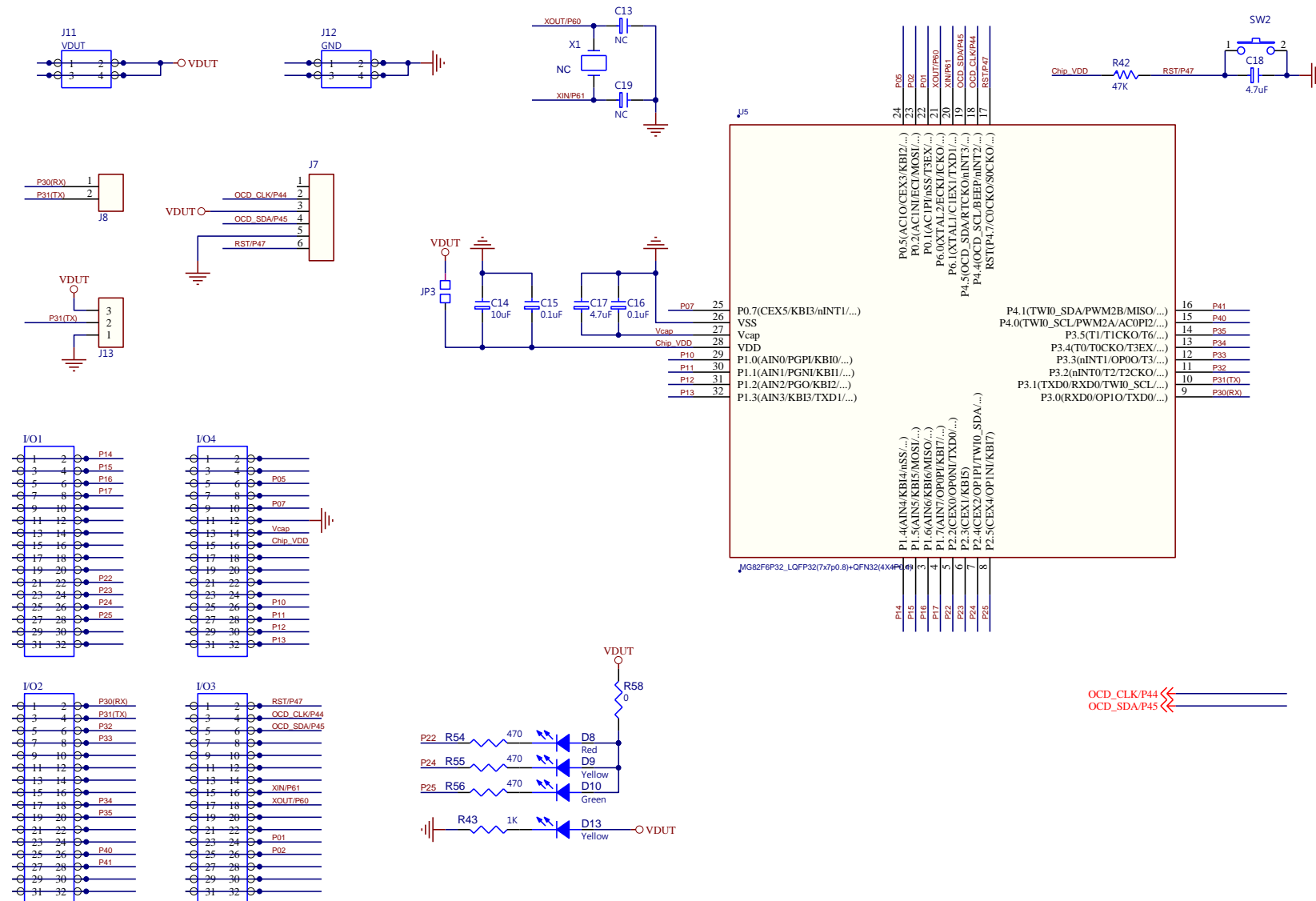


### 1.3 Ev Board Circuit

#### 1.3.1 MLink Circuit

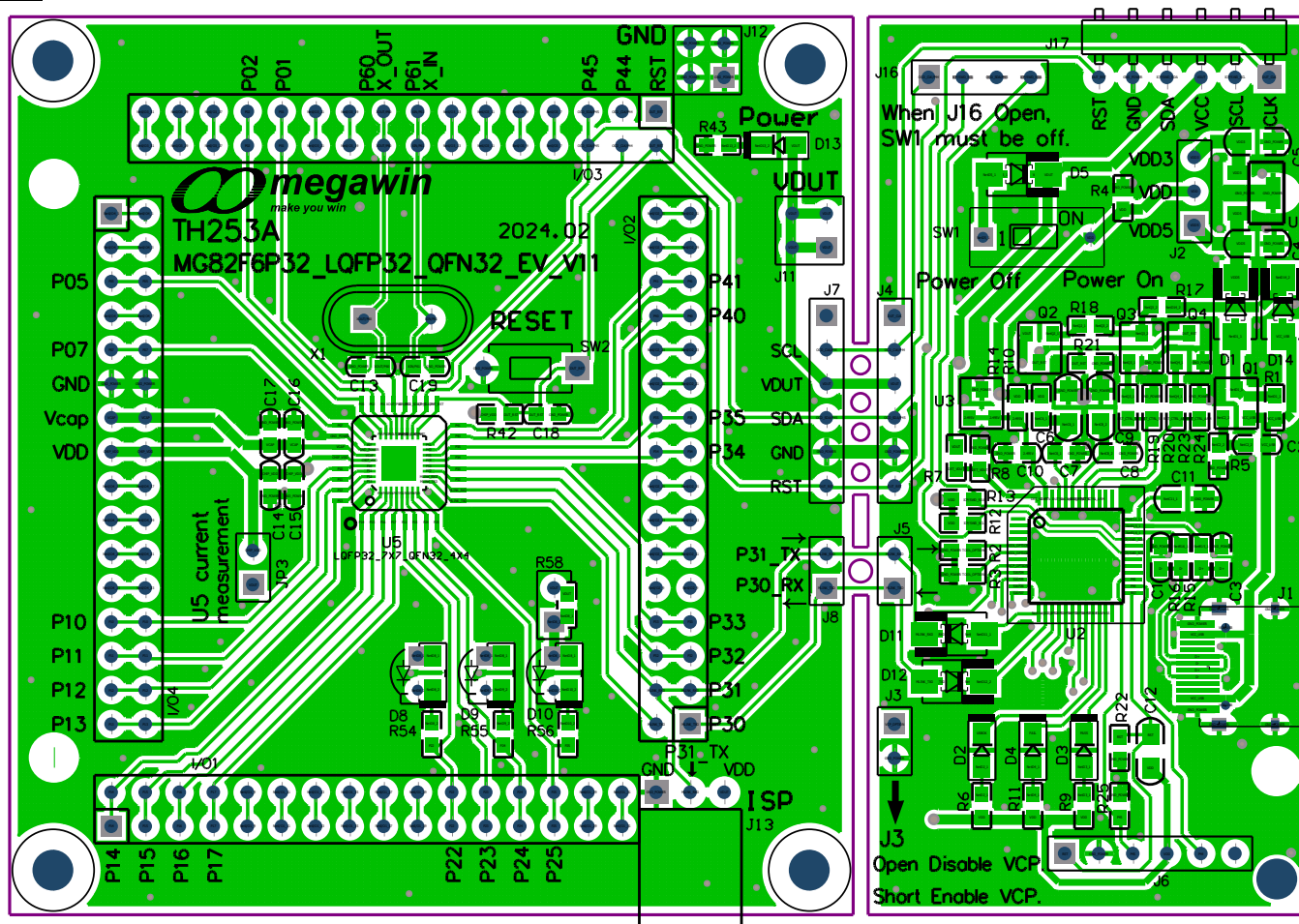


### 1.3.2 MG82F6P32 Circuit

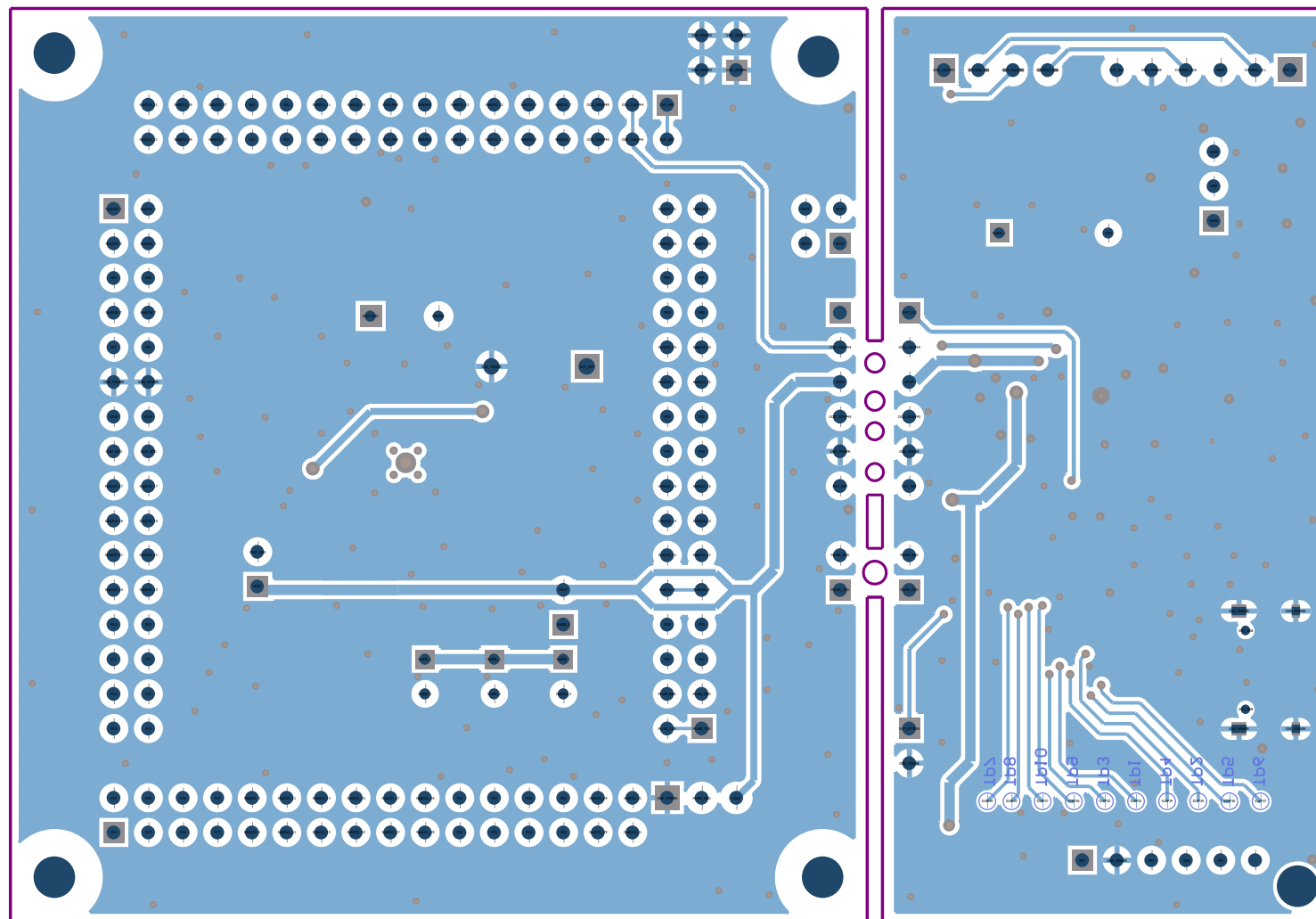


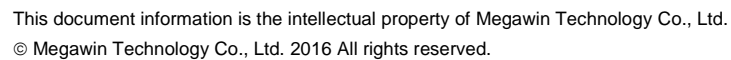
## 1.4 Ev Board PCB

### Top



**Bottom**

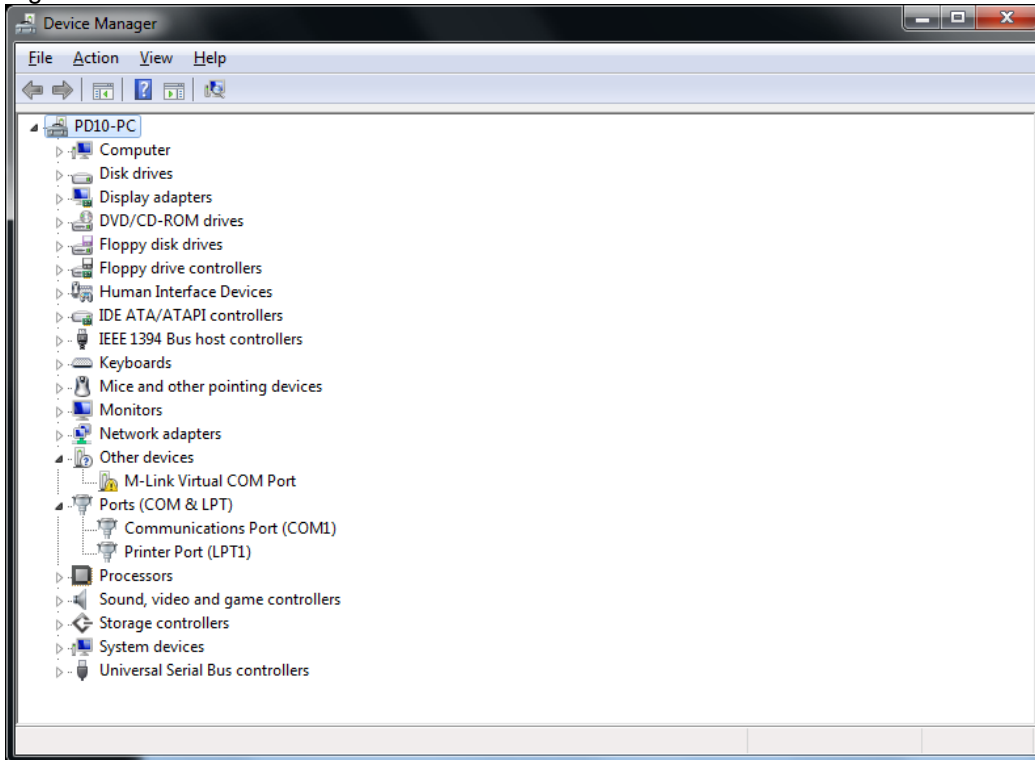




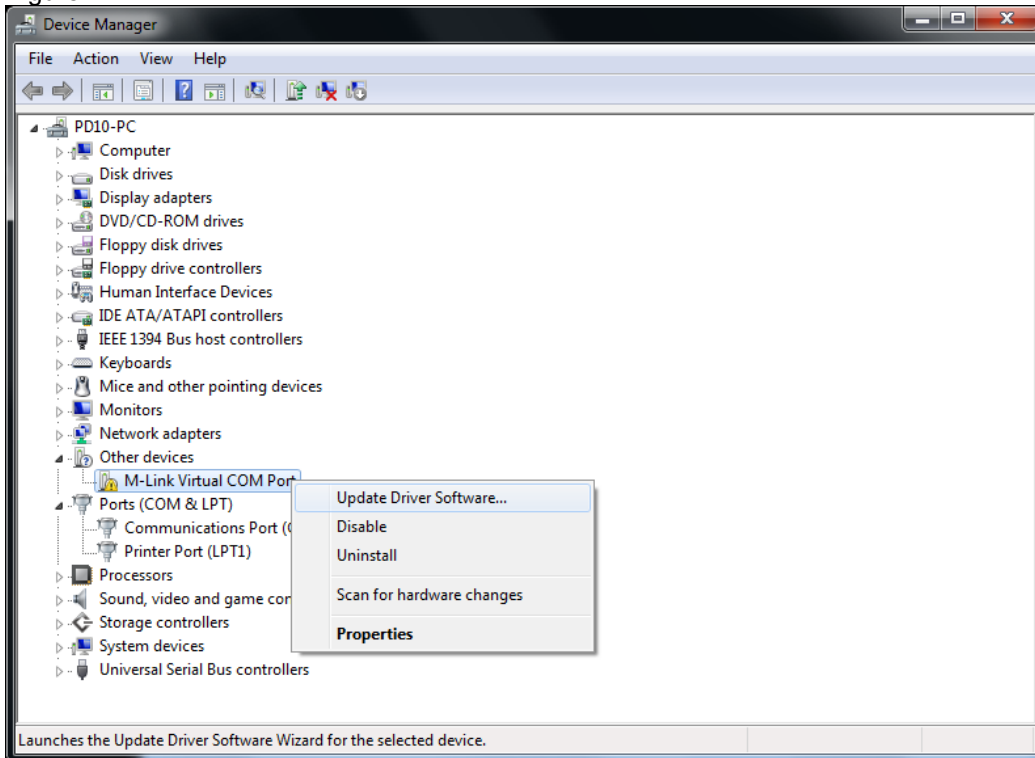


## 2. Driver Install

Step 1: The user short J3 plug MG82F6P32 EV board into any USB port in a PC, then open Device Manager.  
Figure 2-1

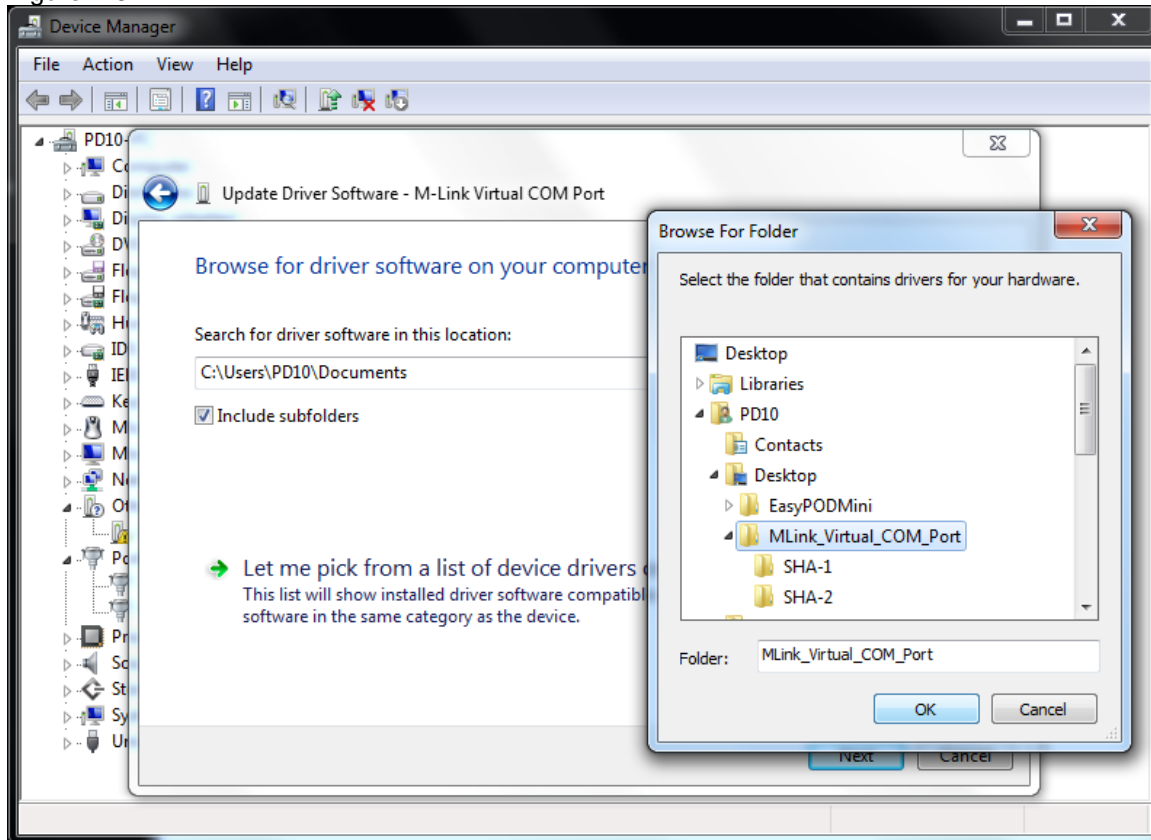


Step 2: Click “Right” key on Megawin MLink Virtual Com Port and “Update Driver Software”...  
Figure 2-2



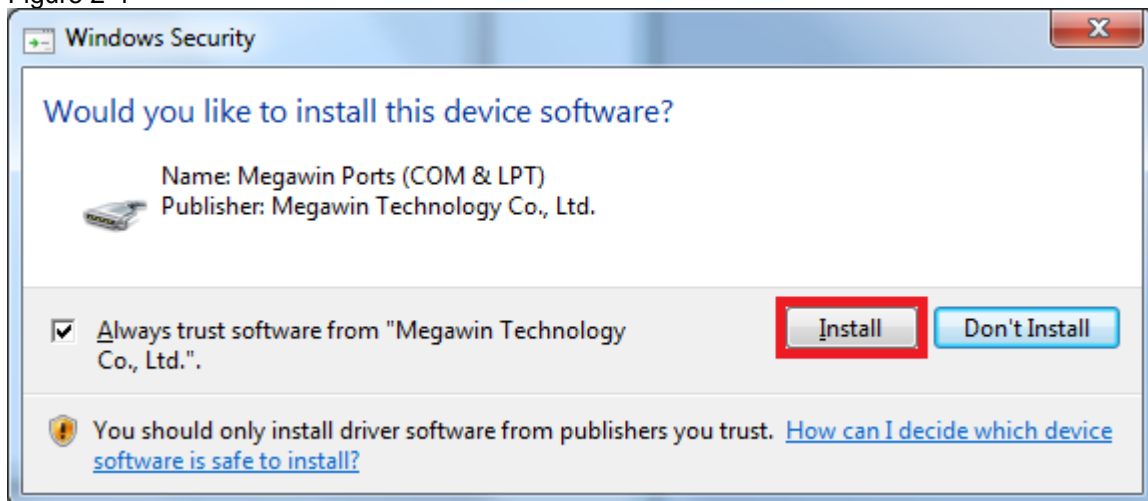
Step 3: Indicate Megawin MLink Virtual Com Port Driver path in the user's PC, OS will select SHA-1 or SHA-2 automatic.

Figure 2-3



Step 4: Click "Install" and wait a while.

Figure 2-4



Step 5: The user install driver successfully...

Figure 2-5

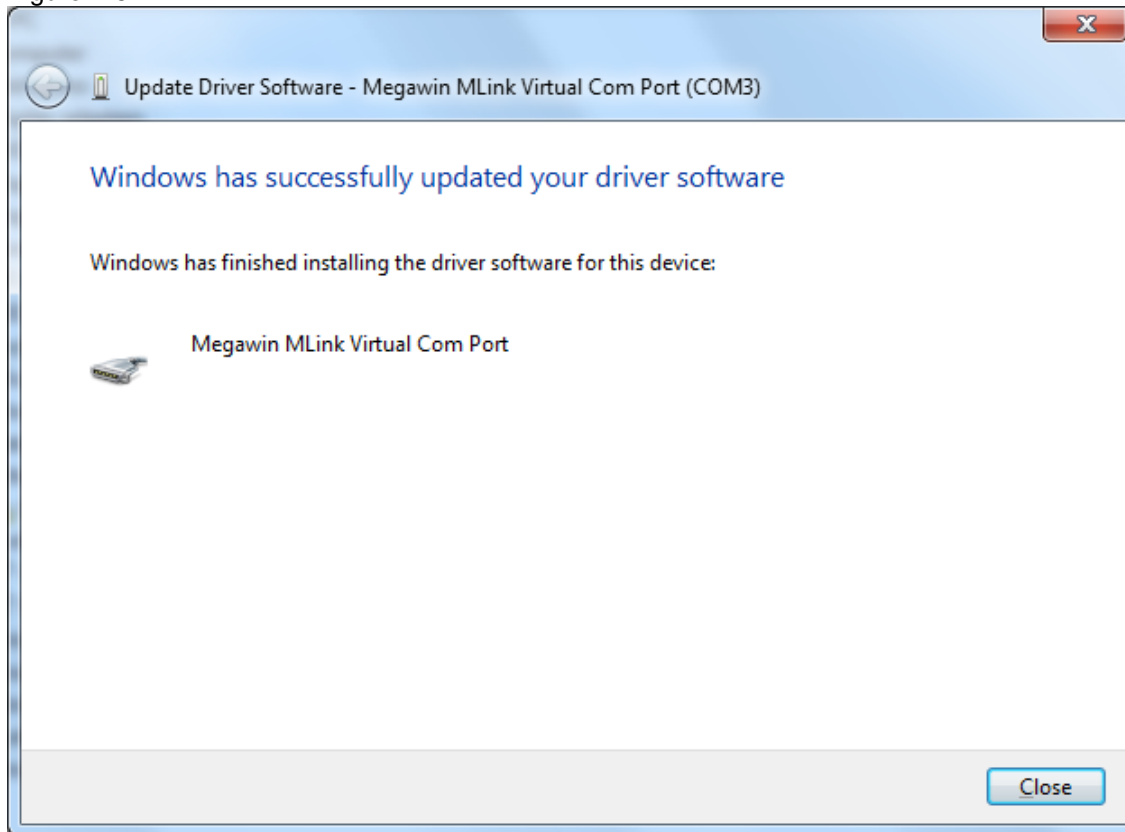
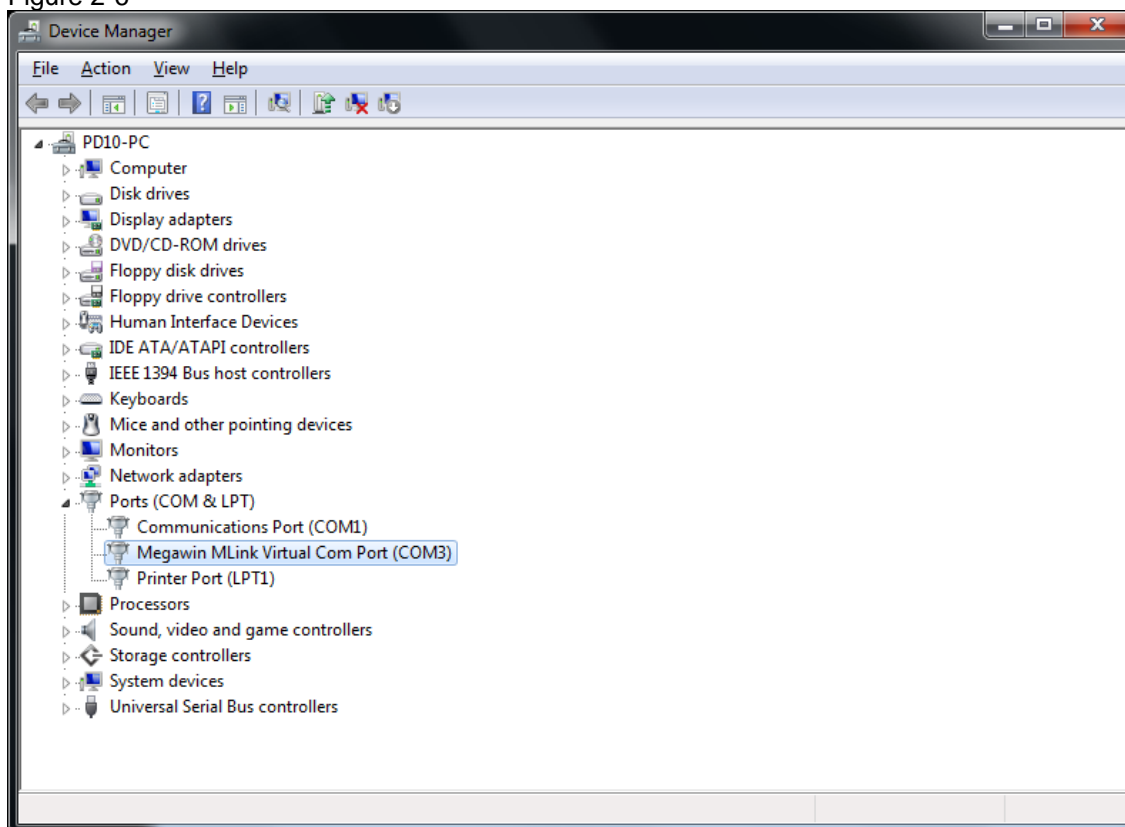


Figure 2-6



### 3. Revision History

Revision	Description	Date
V1.00	(1) New Create.	2024/02/05

## **4. Disclaimers**

Herein, megawin stands for “***megawin Technology Co., Ltd.***”

**Life Support** — This product is not designed for use in medical, life-saving or life-sustaining applications, or systems where malfunction of this product can reasonably be expected to result in personal injury. Customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify Megawin for any damages resulting from such improper use or sale.

**Right to Make Changes** — Megawin reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in mass production, relevant changes will be communicated via an Engineering Change Notification (ECN).